Amendments to the Specification:

Please replace the paragraphs beginning at page 22, line 1, with the following amended paragraphs:

As has already been mentioned above, corresponding control signals C_1, C_2, ... , C_{n-1}, C_n are applied to the control inputs 119a, 119b, 119d, 119e of the gates 116a, 116b, ~~116e,~~ 116d, 116e, namely such that respectively one of the control signals C_1, C_2, ... , C_{n-1}, C_n is in a "logically high" state, and the respectively other control signals C_1, C_2, ... , C_{n-1}, C_n are in a "logically low" state.

In this way, that signal delay element 103a, 103b, 103c, 103d, 103e may be selected whose output signal – possibly in inverted form (namely in the case of signal delay elements 103c, 103d where n is an odd number) – is to be connected through to the output 102b of the signal delay device ~~1~~101.